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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,081	ASANO ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *7 and 8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "the area where at least one of the element and the wire is formed below each of the plurality of thin film resistance elements is identical" (claims 14 and 15) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 14 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 14 and 15, the limitation "wherein the area where at least one of the element and the wire is formed below each of the plurality of thin film resistance elements is identical" renders the claim indefinite. It is unclear what is meant by this limitation. There is only one area defined. Therefore, what is "the area" identical to? Note that claim 15 has a similar problem.

Further regarding claim 14, the limitation "a plurality of the thin film resistance element" should be changed to "a plurality of ~~the~~ thin film resistance elements ~~element~~" (or something similar).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Usami (US Pat. 6,194,775), with Nagao et al. (US PGPub 2001/0053559, hereinafter Nagao) provided as evidence.

Regarding claim 6, Figures 2A-2D of Usami disclose a semiconductor device having a thin film resistance element 209 located above an interlayer insulating film 207 above an area where an element 204 is formed, wherein the interlayer insulating film comprises an inorganic glass film (BPSG) (col. 2, lines 51 and 52) formed so as to cover the overall area below an area where the thin film resistance element is formed. The phrase "spin-on-glass" refers to the manner in which the glass layer is formed. Nagao discloses BPSG is an example of a material that can be deposited by "spin-on" methods (paragraph [0031]). Therefore, the limitation "spin-on-glass" is essentially a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Czagas et al. (US Pat. 6,441,447, hereinafter Czagas).

Regarding claim 1, Figure 3h of Czagas discloses a semiconductor device having a thin film resistance element TFR-2 located above an interlayer insulating film 26 above an area where a wire 22 is formed on a semiconductor substrate 10, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the thin film resistance element is formed intersects to the surface of the semiconductor substrate. Note that the step shown in Figure 3h can be considered "beneath" the area where the resistance element is formed since the term beneath can simply mean "in a lower position". Furthermore, the "area" where the resistance element is formed can be considered to include the entire upper portion (above layer 26) of the device shown in Figure 3h, since the resistive element is formed in that portion. Czagas does not specifically disclose the angle is set to be within a range that is greater than 0 degrees and less than or equal to 10 degrees. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Czagas by using a taper angle less than 10 degrees, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 4, Figure 3h of Czagas discloses the thin film resistance element TFR-2 is formed on an area where the wire 22 is formed. Czagas does not specifically disclose a wire interval is set to 1.7 microns or more. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Czagas by using the claimed wiring interval, since it has been held that discovering an optimum value of a result

effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 5, Figure 3h of Czagas discloses the thin film resistance element TFR-2 is formed above the area where the wire 22 is formed, and the thin film resistance element and the wire are disposed parallel to each other so that projections thereof are overlapped with each other. As can be seen in Figure 3h, layers TFR-2 and 22 overlap. Whatever portions overlap can be considered the projections. The two layers can be considered parallel since the respective planes in which they reside are parallel to each other.

Claims 2, 3, 6, 9, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Czagas in view of Usami, with Nagao provided as evidence.

Regarding claims 2 and 3, Figure 3h of Czagas discloses the interlayer insulating film 26 is formed so as to cover the overall area below the area where the thin film resistance element TFR-2 is formed. A further difference between Czagas and the claimed invention is the interlayer insulating film comprises an inorganic spin-on glass. Figures 2A-2D of Usami disclose an interlayer insulating film made of BPSG below a resistive element 209. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Czagas by using BPSG as the interlayer insulating film for the purpose of selecting a well-known insulating material that has excellent coverage. As stated above, Nagao discloses BPSG is an example of a material that can be deposited by "spin-on" methods (paragraph [0031]). Therefore, the limitation "spin-on-glass" is essentially a product-

by-process limitation that does not structurally distinguish the claimed invention over the prior art. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966.

Further regarding claim 3, Figure 3h of Czagas discloses an upper surface of the interlayer insulating film 26 has a higher area adjacent to an area where the thin film resistance element is formed than in an area where the thin film resistance element is not formed.

Regarding claim 6, Figure 3h of Czagas discloses a semiconductor device having a thin film resistance element TFR-2 located above an interlayer insulating film 26 above an area where a wire 22 is formed, wherein the interlayer insulating film comprises an inorganic glass film (BPSG) (col. 2, lines 51 and 52) formed so as to cover the overall area below an area where the thin film resistance element is formed.

Regarding claim 9, Figure 3h of Czagas discloses a semiconductor device having a thin film resistance element TFR-2 located above an interlayer insulating film 26 above an area where a wire 22 is formed on a semiconductor substrate 10, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the thin film resistance element is formed intersects to the surface of the semiconductor substrate. Note that the step shown in Figure 3h can be considered "beneath" the area where the resistance element is formed since the term beneath can simply mean "in a lower position". Furthermore, the "area" where the resistance element is formed can be considered to include the entire upper portion (above layer 26) of the

device shown in Figure 3h, since the resistive element is formed in that portion. Czagas does not specifically disclose the angle is set to be within a range that is greater than 0 degrees and less than or equal to 10 degrees. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Czagas by using a taper angle less than 10 degrees, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). For the reasons stated above in the rejection of claim 2, it also would have been obvious to use an inorganic spin-on-glass film for the interlayer insulating film. Furthermore, Czagas does not specifically disclose a wire interval is set to 1.7 microns or more. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Czagas by using the claimed wiring interval, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 10 and 11, Czagas does not specifically disclose the resistance element has a width between 1 and 10 microns and a thickness between 10 and 50nm. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Czagas by using the claimed ranges, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Claims 1, 2, 4-6, 9, 10, and 12 are rejected under 35 U.S.C. 103(a) as obvious over Nagao.

Regarding claim 1, Figures 1 and 4 of Nagao discloses a semiconductor device having a thin film resistance element 111 located above an interlayer insulating film (110 or 403) above an area where a wire (107 or 401) is formed on a semiconductor substrate (100 or 400), wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the thin film resistance element is formed intersects to the surface of the semiconductor substrate. Note that pixel electrode 111 inherently has a resistance and therefore can be considered a resistance element. Also note that Nagao discloses the device shown in Figure 1 is formed using the principles shown in Figure 4 (paragraph [0030]), so it also has the step and tapered angle shown in Figure 4. Nagao does not specifically disclose that the taper angle is 10 degrees or less. However, Nagao does disclose it is desirable to improve the flatness (paragraphs [0016] and [0033]). This is supported by the fact that Figure 1 appears to show the insulating film 110 has a completely flat surface. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nagao by using a taper angle less than 10 degrees, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 2, Figure 1 of Nagao discloses the interlayer insulating film 110 comprises an inorganic spin-on-glass (SOG) film (paragraph [0031]) formed so as to cover the overall area below the area where the thin film resistance element is formed.

Regarding claim 4, Figure 1 of Nagao discloses the thin film resistance element 111 is formed on an area where the wire 107 is formed. Figure 4 of Nagao discloses a wire interval of 5-300 microns (based on subtracting "L" from "P", paragraph [0018]), although it is not clear if the same spacing is used for the wires 107 and 108 shown in the device of Figure 1. Therefore, it appears Nagao does not specifically disclose the wire interval is 1.7 microns or more. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the claimed wiring interval, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 5, Figure 1 of Nagao discloses the thin film resistance element 111 is formed above the area where the wire 107 is formed, and the thin film resistance element and the wire are disposed in parallel to each other so that the projections thereof are overlapped with each other. Note the pixel electrode 111 inherently extends in more than one direction. For instance, looking at Figure 1, the electrode 111 also extends into the page, making it parallel to the wire 107. Alternatively, it can be considered that electrode 111 is parallel to wire 107 in the sense that 111 is parallel to the width direction of the wire 107.

Regarding claim 6, Figure 1 of Nagao discloses a thin film resistance element 111 through an interlayer insulating film 110 above an area where a wire 107 is formed, wherein the insulating film comprises an inorganic SOG film (paragraph [0031]) formed so as to cover the overall area below an area where the thin film resistance element is formed.

Regarding claim 9, the claim is essentially a combination of claims 1, 2, and 4. Therefore, the above rejections regarding those claims similarly apply.

Regarding claim 10, Nagao does not specifically disclose the resistance element has a width between 1 and 10 microns and a thickness between 10 and 50nm. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Nagao by using the claimed ranges, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 12, the claim is essentially a combination of claims 1, 2, and 4. Therefore, the above rejections regarding those claims similarly apply. The only difference is that claim 12 recites a plurality of wires. Figure 1 of Nagao discloses a plurality of wires formed on a semiconductor substrate.

Claims 1, 3, 5, 6, and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiiki et al. (US PGPUB 2002/0020879, hereinafter Shiiki) in view of Nagao.

Regarding claim 1, Figure 1A of Shiiki discloses a semiconductor device having a thin film resistance element 2 through an interlayer insulating film 3 above an area where a wire (4 or 6) is formed on a semiconductor substrate. Shiiki does not specifically disclose a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the thin film resistance element is formed intersects to the surface of the semiconductor substrate is set to 10 degrees or less. Figure 4 of Nagao discloses a method of forming an interlayer insulating film 403 over wires 401, wherein

the upper surface of the insulating film has a small step. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Shiiki by using the method of Nagao for the purpose of obtaining a relatively flat surface (paragraph [0033] of Nagao) without requiring any additional planarization steps, such as CMP. Note that Shiiki discloses using CMP to flatten the interlayer insulating film (see abstract). It is known in the art that CMP has many drawbacks, including high cost. Therefore, eliminating that step would reduce the cost and simplify the production process. A further difference between Shiiki and the claimed invention is the taper angle is less than 10 degrees. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify Shiiki and Nagao by using a taper angle less than 10 degrees, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 3, since the step in the insulating film is formed as a result of the underlying wiring 6, and that wiring is located under the resistance element, it follows that an upper surface of the interlayer insulating film has a higher area adjacent to an area where the thin film resistance element is formed than in an area where the resistance element is not formed (see Figures 1A and 1B of Shiiki). It is further obvious to use the inorganic SOG film of Nagao (paragraph [0031]) for the purpose of using an insulating material that can function as a good leveling film.

Regarding claim 5, Figure 1A of Shiiki discloses the thin film resistance element 2 is formed above the area where the wire (4 or 6) is formed, and the thin film resistance element and the wire are disposed in parallel to each other so that projections thereof are overlapped with

each other. Figure 1A of Shiiki shows layers 2 and 4 (or 6) overlap. Whatever portions overlap can be considered the projections. The two layers can be considered parallel since the respective planes in which they reside are parallel to each other.

Regarding claim 6, Figure 1A of Shiiki discloses a thin film resistance element 2 through an interlayer insulating film 3 above an area where a wire 4 is formed, wherein the film is formed to cover the overall area below an area where the thin film resistance element is formed. It is obvious to use the inorganic SOG film of Nagao (paragraph [0031]) for the purpose of using an insulating material that can function as a good leveling film.

Regarding claims 9 and 12, the rejection of claims 1 and 3 set forth above similarly applies to these claims. Regarding claim 12, Figure 1A of Shiiki discloses a plurality of wires 4. A further difference between Shiiki and the claimed invention is a wire interval is set to 1.7 microns or more. It would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the invention of Shiiki by using the claimed wire interval range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. It would have been obvious to use a wire interval of 1.7 microns or more to reduce the parasitic capacitance between the wires.

Regarding claims 10 and 11, Shiiki discloses the thin film resistance element 2 is formed to have a thickness of 500 angstroms (50nm) (paragraph [0052]), which is within the claimed range of 10-50 nm. Shiiki does not specifically disclose the resistance element has a width between 1 and 10 microns. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the invention of Shiiki by using the

claimed width range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 13, Figures 1A and 1B of Shiiki disclose the thin film resistance element 2 further comprises paired thin film resistance elements 2. Note that Figure 1B shows two resistance elements 2 connected by an electrode 1. These resistance elements can be considered "paired".

Response to Arguments

Applicant's arguments filed 1/30/2006 and 2/14/2006 have been fully considered but they are not persuasive.

Applicant argues that the pixel electrode 111 of Nagao cannot be a resistive element and that the Examiner's contention is "completely unreasonable". Note that Applicant does not claim a resistor, but instead claims a resistance element. As stated previously, element 111 of Nagao can be considered a resistance element since it inherently has at least some resistance. If Applicant can state for the record that element 111 of Nagao has absolutely no resistance, the Examiner will withdraw this interpretation. Note that Applicant has not defined the degree of resistivity an element must have in order to be considered resistive. Applicant further argues, regarding the combination of Shiiki and Nagao, that the ordinary artisan would not have been motivated to combine the references because "The purpose of the flattening performed in Nagao et al. is to improved the wire reliability, orientation control of the liquid crystal and reflectance fo

the display device." Simply because Nagao performs the flattening operation for one reason does not mean the flattening operation cannot be carried out for different reason. In the Final Rejection, the Examiner provided a specific motivational statement as to why the ordinary artisan would have been motivated to combine the references. Obtaining a flat surface for subsequent layer deposition would be advantageous regardless of the specific type of device. Applicant further argues (in the response filed 2/14/2006) that Shiiki teaches an alternative to use of CMP (SOG followed by etchback). Simply because Shiiki discloses a different way to level the surface doesn't mean the stated motivation for the combination is invalid. The point of the 103 rejection was to eliminate the need for any subsequent leveling step. CMP was simply cited as an example.

Applicant further argues "According to Shiiki, the 100-500 angstrom resistive film has a region in which an error output by the ladder circuit or the pair property deteriorates (5%-17% pair dispersion". It is unclear how this argument overcomes the rejection since Shiiki specifically discloses a thickness value (50nm) within the claimed range. The thickness of the resistance element is not what has been modified.

Applicant further argues that "In Figs. 2A and 3C, the applicants clearly show the superior results achieved by the recited taper angel and metal fin space, respectively." It is initially noted that the claims do not recite a specific metal fin space. Further, Applicant must show that any allegedly superior results are unexpected. The evidence relied should establish "that the differences in results are in fact unexpected and unobvious and of both statistical and practical significance." Ex parte Gelles, 22 USPQ2d 1318, 1319 (Bd. Pat. App. & Inter. 1992). Figures 2A and 3C merely show various data points based on Applicant's invention. The data

does not show that the results are unexpected. It should be noted that the claimed range is essentially provides that the interlayer insulating film is flat, but not completely flat. If it were completely flat, the angle would be 0 degrees. The device of Nagao is clearly not completely flat (as shown in Figure 4), but it would certainly be obvious modify Nagao to have the surface as flat as possible (i.e., less than 10 degrees). The benefits of obtaining a flat surface would not be unexpected as apparently alleged by Applicant. Where the unexpected properties of a claimed invention are not shown to have a significance equal to or greater than the expected properties, the evidence of unexpected properties may not be sufficient to rebut the evidence of obviousness. In re Nolan, 553 F.2d 1261, 1267, 193 USPQ 641, 645 (CCPA 1977). Furthermore, Applicant has not compared the allegedly superior results with the closest prior art. An affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. In re Burckel, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979). It is further noted that Figure 2A shows data points with a best fit line connecting those data points. However, there is no data point at the 10 degree mark. Therefore, Applicant has not shown that the allegedly superior results are commensurate in scope with the claim limitation "greater that 0° and less than or equal to 10°". In other words, Figure 2A does not show the criticality of 10°.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew C. Landau

April 17, 2006